IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

please enter
02/23/04
VN

In re application: **Weber**	§	
Serial No.: **09/993,015**	§	Group Art Unit: **2829**
Filed: **November 5, 2001**	§	Examiner: **Nguyen, Vinh P.**
For: **Method and Apparatus for Automatic Marking of Integrated Circuits in Wafer Scale Testing**	§	Attorney Docket No.: **01-379**

Certificate of Transmission Under 37 C.F.R. § 1.8(a)
I hereby certify this correspondence is being transmitted via facsimile to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, facsimile number (703) 872-9306, on February 9, 2004.
By: Amelia C. Turner
Amelia C. Turner

RESPONSE TO FINAL OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

No fees are believed to be required. If, however, any fees are required, I authorize the Commissioner to charge these fees which may be required to LSI Logic Corporation Deposit Account No. 12-2252. No extension of time is believed to be necessary. If, however, an extension of time is required, the extension is requested, and I authorize the Commissioner to charge any fees for this extension to LSI Logic Corporation Deposit Account No. 12-2252.

In response to the Final Office Action dated December 9, 2003, please amend the above-identified application as follows: